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EXAMINER

LEVIN, NAUM B

ART UNIT

PAPER NUMBER

2825

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PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

|                              |                                      |                                       |  |
|------------------------------|--------------------------------------|---------------------------------------|--|
| <b>Office Action Summary</b> | <b>Application No.</b><br>10/604,964 | <b>Applicant(s)</b><br>HOSSAIN, RAZAK |  |
|                              | <b>Examiner</b><br>NAUM B. LEVIN     | <b>Art Unit</b><br>2825               |  |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 07 May 2008.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-3 and 20-36 is/are pending in the application.
- 4a) Of the above claim(s) 1-3 and 33 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 20-32 and 34-36 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

### DETAILED ACTION

1. This office action is in response to application 10/604,964, RCE filed on 12/03/2007 and Response to election/restriction filed on 05/07/08. Applicant has provisionally elected claims 20-32, 34-36 (Group 2) with traverse. Claims 1-3 and 33 (Group 1) are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected and must be cancelled. Claims 1-3 and 20-36 remain pending in the Application.

2. The possible invention of Group 1 is related to configuration vector for routing connections between circuit elements to reduce leakage current in a circuit, the possible invention of Group 2 is related to select between test vector and configuration vector to test a circuit, thereby Group 2 includes separate utilities such as: selecting between test vector and configuration vector; selecting between test vector enable signal and configuration vector enable signal. Applicant's specification also distinguishes these groups. For example, in paragraphs 13-14 the specification recites configuration **vector that applies in a sleep mode** and configures the circuit elements into a state **in which leakage currents are minimized**. Another embodiment discloses a test vector, wherein the **test vector is applied in a test mode** (paragraph 20).

3. Because these inventions are independent or distinct for the reasons given above and there would be a serious burden on the examiner if restriction is not required, because the inventions have acquired a separate status in the art in view of their different classification that requires a different field of search (see MPEP § 808.02), restriction for examination purposes as indicated is proper.

As such, the restriction is hereby made final.

### ***Response to Amendment***

4. The evidence submitted is insufficient to establish a conception of the invention prior to the effective date of the Abdollahi's reference. While conception is the mental part of the inventive act, it must be capable of proof, such as by demonstrative evidence or by a complete disclosure to another. Conception is more than a vague idea of how to solve a problem. The requisite means themselves and their interaction must also be comprehended. See *Mergenthaler v. Scudder*, 1897 C.D. 724, 81 O.G. 1417 (D.C. Cir. 1897). Particularly, attached sketches do not exhibit, for example, such important elements as clock generator 40 and vector memory 37 as shown in Fig.1 of the Applicant's disclosure. Also see MPEP § 715 .07.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 20, 23, 32 and 34 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification does not recite following limitation of above claims: the

multiplexer/device that is configured to **select between the configuration vector and the test vector.**

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 23 and 32 are recites the limitation "said first selected vector" and "said second selected vector" in lines 11, 13 accordingly. There is insufficient antecedent basis for this limitation in the claim.

### ***Claim Objections***

7. Claims 20, 23, 32 and 34 are objected to because following informalities:

Applicant must clarify what are "circuit elements" and "selective application".

Appropriate corrections are required.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

8. Claims 20-32, 34-36 are rejected under 35 U.S.C. 102(a) as being unpatentable by Abdollahi et al. ("Leakage current reduction in sequential circuits by modifying the scan chains", fourth international symposium on 24-28 March 2003").

9. As to claims 20, 23, 32 and 34 Abdollahi discloses:

**Claim 20 A circuit comprising:**

**circuit elements** (The scan chain applies the test data to various circuit elements, which produce a known output if operating correctly – Applicant's specification, paragraph 5) (As best understood, scan-chains that are already put into the circuit in order to allow efficient testing of the circuit elements functionality – page 50, left col., lines 1-2);

**scan chain elements to contain a vector for selective application** (a configuration vector which, when applied to the circuit elements, configures the circuit elements into a state in which a leakage current is reduced. A multiplexer selects the configuration vector for loading into the scan chain elements - Applicant's specification, paragraph 13) to said circuit elements (As best understood, when the sleep signal is high, the current state will be saved in the added flip-flops; at the same time the MLV/minimum leakage vector/selective application is loaded/contain into the multiplexed-input flip-flops/scan chain elements driving the inputs of the combinational circuit/circuit elements – page 53, left col., lines 1-10);

**a vector memory for containing a configuration vector** (memory implemented as  $(m+k)$ -bit shift register that is used for storing the *MLV* – page 52, left col., lines 8-18; Fig.6) **which, when applied to said circuit elements** (the method to apply the *MLV* to

the circuit - page 52, left col., lines 45-51; page 52, right col., lines 1-6), **configures said circuit elements into a state in which a leakage current is reduced** (This method over writes the previous state of the circuit/configures circuit elements into a state with the *MLV/minimum leakage vector to reduce a leakage current/* in which a leakage current is reduced - page 52, right col., lines 6-7);

**a multiplexer to select said configuration vector for loading into said scan chain elements** (page 52, left col., lines 45-51; page 52, right col., lines 1-6; Fig.7);

**a clock generator to clock said configuration vector into said scan chain elements** (to shift in the *MLV/to clock configuration vector*, from a memory ( $m+k$  bit shift register) into the first  $m+k$  flip-flops/into scan chain via the *ScanIn* pin by setting the circuit into the test mode and applying  $m+k$  clocks/clock generating. For this reason the sleep signal, generated by the power management unit, is combined with the test signal to construct the new control input of the multiplexed flip-flops. After shifting in the MLV, the clock signal/clock generator can be disabled to avoid power dissipation in the flip-flops as depicted in Figure 5 - page 51, right col., lines 17-24; page 54, left col., lines 1-11; Fig.5; Fig. 13);

**a circuit for receiving a test vector for clocking into said scan chain elements** (to apply a test vector the circuit is set into test mode/a circuit for receiving a test vector by setting *test=0* and shifting/clocking the test vector into flip-flops/ scan chain elements via *ScanIn* pin by applying  $m+k$  clocks, where  $m$  and  $k$  are the number of input and internal flip-flops, respectively. This causes the test vector be applied to the primary inputs of the circuit - page 51, left col., lines 31-50; Fig.4);

**wherein said multiplexer is configured to select between said configuration vector and said test vector for loading into said scan chain elements** (As best understood, the multiplexer that provide output signal to flip-flops is configured such as to shift/select the MLV/configuration vector into the first  $m+k$  flip-flops/scan chain elements. For this reason the sleep signal, generated by the power management unit, is combined with the test signal to construct the new control input/replace test signal of the multiplexed flip-flops - page 51, right col., lines 10-22; page 52, left col., lines 45-51; page 52, right col., lines 1-11; Figs.5, 7-8); **and**

**wherein said clock generator is configured to clock said selected vector into said scan elements** (page 51, right col., lines 17-24; page 54, left col., lines 1-11; Fig.5; Figs. 9, 13);

**Claim 23 A circuit comprising:**

**circuit elements** (The scan chain applies the test data to various circuit elements, which produce a known output if operating correctly – Applicant's specification, paragraph 5) (As best understood, scan-chains that are already put into the circuit in order to allow efficient testing of the circuit elements functionality – page 50, left col., lines 1-2);

**scan chain elements to contain a vector for selective application** (a configuration vector which, when applied to the circuit elements, configures the circuit elements into a state in which a leakage current is reduced. A multiplexer selects the configuration vector for loading into the scan chain elements - Applicant's specification, paragraph 13) to said circuit elements (As best understood, when the sleep signal is



high, the current state will be saved in the added flip-flops; at the same time the MLV/minimum leakage vector/selective application is loaded/contain into the multiplexed-input flip-flops/scan chain elements driving the inputs of the combinational circuit/circuit elements – page 53, left col., lines 1-10);

**a test input for receiving a test vector** (to apply a test vector the circuit is set into test mode/a circuit for receiving a test vector by setting  $test=0$  and shifting/clocking the test vector into flip-flops/ scan chain elements via *ScanIn* pin by applying  $m+k$  clocks. This causes the test vector be applied to the primary inputs of the circuit - page 51, left col., lines 31-50; Fig.4);

**a vector memory for containing a configuration vector** (memory implemented as  $(m+k)$ -bit shift register that is used for storing the *MLV* – page 52, left col., lines 8-18; Fig.6) **which, when applied to said circuit elements** (the method to apply the *MLV* to the circuit - page 52, left col., lines 45-51; page 52, right col., lines 1-6), **configures said circuit elements into a state in which a leakage current is reduced** (This method over writes the previous state of the circuit/configures circuit elements into a state with the MLV/minimum leakage vector to reduce a leakage current/ in which a leakage current is reduced - page 52, right col., lines 6-7);

**a first multiplexer to select between said configuration vector and said test vector for loading into said scan chain elements** (As best understood (the multiplexer that provide output signal to flip-flops is configured such as to shift/select the MLV/configuration vector into the first  $m+k$  flip-flops/scan chain elements. For this reason the sleep signal, generated by the power management unit, is combined with the

test signal to construct the new control input/replace test signal of the multiplexed flip-flops - page 51, right col., lines 10-22; page 52, left col., lines 45-51; page 52, right col., lines 1-11; Figs.5, 7-8);

**a second multiplexer to select between a test enable signal and a configuration vector enable signal and output a selected enable signal, said selected enable signal operable for enabling said scan chain elements to select between said first selected vector and a normal operation mode data vector for loading into said scan chain elements** (to apply  $m+k$  new multiplexers are inserted in the scan chain, in such a way that each output of a flip-flop in the scan chain is multiplexed with the corresponding minimum leakage value and the output of the multiplexer is connected to the  $DS$  input of the next multiplexed-input flip-flop as depicted in Figure 7 – page 52, left col., last paragraph; The test signal needs to be set to *one* whenever the circuit enters the sleep mode - page 52, right col., lines 1-2; This method over writes the previous state/normal mode of the circuit with the  $MLV$ . To solve this problem we add  $m+k$  flip-flops and multiplexers controlled by the sleep signal to the circuit, which are used to save the  $MLV$  in the active mode and the previous state in the sleep mode. For this reason we construct a local loop corresponding to each input as shown in Figure 8 - page 52, right col., lines 6-11; page 53, left col., lines 1-10; Figs.7-9; 11-13); **and**

**a clock generator to clock said second vector into said scan chain elements** (As best understood, to shift in the  $MLV$ /to clock configuration vector, from a memory ( $m+k$  bit shift register) into the first  $m+k$  flip-flops/into scan chain via the *ScanIn*

pin by setting the circuit into the test mode and applying  $m+k$  clocks/clock generating.

For this reason the sleep signal, generated by the power management unit, is combined with the test signal to construct the new control input of the multiplexed flip-flops. After shifting in the MLV, the clock signal/clock generator can be disabled to avoid power dissipation in the flip-flops as depicted in Figure 5 - page 51, right col., lines 17-24; page 54, left col., lines 1-11; Fig.5; Fig. 13);

**Claim 32 A circuit comprising:**

**circuit elements** (The scan chain applies the test data to various circuit elements, which produce a known output if operating correctly – Applicant's specification, paragraph 5) (As best understood, scan-chains that are already put into the circuit in order to allow efficient testing of the circuit elements functionality – page 50, left col., lines 1-2);

**scan chain elements to contain a vector for selective application** (a configuration vector which, when applied to the circuit elements, configures the circuit elements into a state in which a leakage current is reduced. A multiplexer selects the configuration vector for loading into the scan chain elements - Applicant's specification, paragraph 13) **to said circuit elements** (As best understood, when the sleep signal is high, the current state will be saved in the added flip-flops; at the same time the MLV/minimum leakage vector/selective application is loaded/contain into the multiplexed-input flip-flops/scan chain elements driving the inputs of the combinational circuit/circuit elements – page 53, left col., lines 1-10);

**means for receiving a test vector** (to apply a test vector the circuit is set into test mode/a circuit for receiving a test vector by setting  $test=0$  and shifting/clocking the test vector into flip-flops/ scan chain elements via *ScanIn* pin by applying  $m+k$  clocks. This causes the test vector be applied to the primary inputs of the circuit - page 51, left col., lines 31-50; Fig.4);

**means for storing a configuration vector** (memory implemented as  $(m+k)$ -bit shift register that is used for storing the *MLV* – page 52, left col., lines 8-18; Fig.6)  
**which, when applied to said circuit elements** (the method to apply the *MLV* to the circuit - page 52, left col., lines 45-51; page 52, right col., lines 1-6), **configures said circuit elements into a state in which a leakage current is reduced** (This method over writes the previous state of the circuit/configures circuit elements into a state with the *MLV/minimum leakage vector to reduce a leakage current/* in which a leakage current is reduced - page 52, right col., lines 6-7);

**means for selecting between said configuration vector and said test vector for loading into said scan chain elements** (As best understood (the multiplexer that provide output signal to flip-flops is configured such as to shift/select the *MLV/configuration vector* into the first  $m+k$  flip-flops/scan chain elements. For this reason the sleep signal, generated by the power management unit, is combined with the test signal to construct the new control input/replace test signal of the multiplexed flip-flops - page 51, right col., lines 10-22; page 52, left col., lines 45-51; page 52, right col., lines 1-11; Figs.5, 7-8);

**means for a second multiplexer to select between a test enable signal and a configuration vector enable signal and output a selected enable signal, said selected enable signal operable for enabling said scan chain elements to select between said first selected vector and a normal operation mode data vector for loading into said scan chain elements** (to apply  $MLV\ m+k$  new multiplexers are inserted in the scan chain, in such a way that each output of a flip-flop in the scan chain is multiplexed with the corresponding minimum leakage value and the output of the multiplexer is connected to the  $DS$  input of the next multiplexed-input flip-flop as depicted in Figure 7 – page 52, left col., last paragraph; The test signal needs to be set to *one* whenever the circuit enters the sleep mode - page 52, right col., lines 1-2; This method over writes the previous state/normal mode of the circuit with the  $MLV$ . To solve this problem we add  $m+k$  flip-flops and multiplexers controlled by the sleep signal to the circuit, which are used to save the  $MLV$  in the active mode and the previous state in the sleep mode. For this reason we construct a local loop corresponding to each input as shown in Figure 8 - page 52, right col., lines 6-11; page 53, left col., lines 1-10; Figs.7-9; 11-13); **and**

**means for generating a clocking signal to clock said second vector into said scan chain elements** (to shift in the  $MLV$ /to clock configuration vector, from a memory ( $m+k$  bit shift register) into the first  $m+k$  flip-flops/into scan chain via the  $ScanIn$  pin by setting the circuit into the test mode and applying  $m+k$  clocks/clock generating. For this reason the sleep signal, generated by the power management unit, is combined with the test signal to construct the new control input of the multiplexed flip-flops. After

shifting in the MLV, the clock signal/clock generator can be disabled to avoid power dissipation in the flip-flops as depicted in Figure 5 - page 51, right col., lines 17-24; page 54, left col., lines 1-11; Fig.5; Fig. 13);

**Claim 34 A circuit comprising:**

**providing circuit elements** (The scan chain applies the test data to various circuit elements, which produce a known output if operating correctly – Applicant's specification, paragraph 5) (As best understood, scan-chains that are already put into the circuit in order to allow efficient testing of the circuit elements functionality – page 50, left col., lines 1-2);

**providing scan chain elements to contain a vector for selective application** (a configuration vector which, when applied to the circuit elements, configures the circuit elements into a state in which a leakage current is reduced. A multiplexer selects the configuration vector for loading into the scan chain elements - Applicant's specification, paragraph 13) to said circuit elements (As best understood, when the sleep signal is high, the current state will be saved in the added flip-flops; at the same time the MLV/minimum leakage vector/selective application is loaded/contain into the multiplexed-input flip-flops/scan chain elements driving the inputs of the combinational circuit/circuit elements – page 53, left col., lines 1-10);

**receiving a configuration vector from a memory** (m input flip-flops receive MLV /configuration vector from memory; memory implemented as  $(m+k)$ -bit shift register that is used for storing the MLV – page 52, left col., lines 8-18; Fig.6) which, when applied to said circuit elements (the method to apply the MLV to the circuit - page 52,

left col., lines 45-51; page 52, right col., lines 1-6), **configures said circuit elements into a state in which a leakage current is reduced** (This method over writes the previous state of the circuit/configures circuit elements into a state with the MLV/minimum leakage vector to reduce a leakage current/ in which a leakage current is reduced - page 52, right col., lines 6-7);

**selecting between said configuration vector and said test vector for loading into said scan chain elements (As best understood** (the multiplexer that provide output signal to flip-flops is configured such as to shift/select the *MLV/configuration vector* into the first  $m+k$  flip-flops/scan chain elements. For this reason the sleep signal, generated by the power management unit, is combined with the test signal to construct the new control input/replace test signal of the multiplexed flip-flops - page 51, right col., lines 10-22; page 52, left col., lines 45-51; page 52, right col., lines 1-11; Figs.5, 7-8);

**selecting between a test enable signal and a configuration vector enable signal and outputting a first selected vector, selecting between a test enable signal and a configuration vector enable signal and outputting a selected enable signal** (to apply *MLV  $m+k$*  new multiplexers are inserted in the scan chain, in such a way that each output of a flip-flop in the scan chain is multiplexed with the corresponding minimum leakage value and the output of the multiplexer is connected to the DS input of the next multiplexed-input flip-flop as depicted in Figure 7 – page 52, left col., last paragraph; The test signal needs to be set to one whenever the circuit enters the sleep mode - page 52, right col., lines 1-2; This method over writes the previous state/normal mode of the circuit with the *MLV*. To solve this problem we add  $m+k$  flip-

flops and multiplexers controlled by the sleep signal to the circuit, which are used to save the *MLV* in the active mode and the previous state in the sleep mode. For this reason we construct a local loop corresponding to each input as shown in Figure 8 - page 52, right col., lines 6-11; page 53, left col., lines 1-10; Figs.7-9; 11-13);

**receiving said selected enable signal and said first selected vector, and in response thereto, selecting between said first selected vector and a normal operation mode data vector for loading into said scan chain elements** (page 52, right col., lines 6-11; page 53, left col., lines 1-10; Figs.7-9; 11-13); **and**

**generating a clocking signal to clock said vector selected by said selected enable signal into said scan chain elements and applying said clocked vector to said circuit elements** (to shift in the *MLV*/to clock configuration vector, from a memory ( $m+k$  bit shift register) into the first  $m+k$  flip-flops/into scan chain via the *ScanIn* pin by setting the circuit into the test mode and applying  $m+k$  clocks/clock generating. For this reason the sleep signal, generated by the power management unit, is combined with the test signal to construct the new control input of the multiplexed flip-flops. - page 51, right col., lines 17-24; page 54, left col., lines 1-11; Figs.5, 7-9, 11-13).

10. As to claims 21-22, 24-31 and 35-36 Abdollahi recites:

**Claims 21, 24, 35 The circuit/method further comprising a sleep mode**  
(Abstract; page 50, right col., lines 3-12);

**Claims 22, 25-26, 28-30. 36 The circuit/method further comprising a scan chain turn off circuit to turn off a clock to said scan chain elements after said configuration vector has been applied to said circuit elements** (pages 51-53);



**Claim 27** The circuit, wherein during a sleep mode, said configuration vector enable signal is activated for a predetermined number of cycles equal to or less than the number of said scan chain elements (page 51, right col., lines 10-25);

**Claim 31** The circuit, wherein said configuration vector comprises at least two data and each data in said configuration vector is sequentially loaded into said scan chain elements in response to said clocking signal (page 54, left col., lines 1-11; Fig.13).

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NAUM B. LEVIN whose telephone number is (571)272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Naum Levin/  
Examiner  
Art Unit 2825